CLAIMS

What is claimed is:

1. A semiconductor circuit fuse, comprising:

an insulating substrate;

a refractory metal nitride layer disposed above the insulating substrate; and

a tungsten silicide layer disposed over the refractory metal nitride layer.

2. The semiconductor circuit fuse of claim 1, wherein the insulating substrate is an isolation region.

3. The semiconductor circuit fuse of claim 2, wherein the isolation region is a field oxide region.

4. The semiconductor circuit fuse of claim 3, wherein the field oxide region is disposed on a semiconductor substrate.

5. The semiconductor circuit fuse of claim 4, wherein the semiconductor substrate is a silicon wafer.

6. The semiconductor circuit fuse of claim 1, wherein the refractory metal nitride layer and the tungsten silicide layer are configured to a similar shape.

7. The semiconductor circuit fuse of claim 6, wherein the similar shape comprises a neck portion located between terminal portions.

8. The semiconductor circuit fuse of claim 7, wherein the neck portion is smaller in width than the terminal portions.

9. The semiconductor circuit fuse of claim 8, wherein the neck portion has a width within a range of about 0.2 to about 1 micron.

10. The semiconductor circuit fuse of claim 9, wherein the width of the neck portion is about 0.35 microns.

11. The semiconductor circuit fuse of claim 9, wherein a length of the neck portion is within a range of about 1 to about 10 microns.

12. The semiconductor circuit fuse of claim 11, wherein the length of the neck portion is about 3.5 microns.

13. The semiconductor circuit fuse of claim 1, wherein the refractory metal nitride layer comprises titanium nitride.

14. A semiconductor circuit fuse, comprising:
an insulating substrate;
a refractory metal nitride layer disposed above the insulating substrate; and
a conductive layer disposed over the refractory metal nitride layer.

15. The semiconductor circuit fuse of claim 14, wherein the insulating substrate is an isolation region.

16. The semiconductor circuit fuse of claim 15, wherein the isolation region is a field oxide region.

17. The semiconductor circuit fuse of claim 16, wherein the field oxide region is disposed on a semiconductor substrate.

18. The semiconductor circuit fuse of claim 17, wherein the semiconductor substrate is a silicon wafer.

19. The semiconductor circuit fuse of claim 14, wherein the refractory metal nitride layer includes titanium.

20. The semiconductor circuit fuse of claim 14, wherein the refractory metal nitride layer comprises titanium nitride.

21. The semiconductor circuit fuse of claim 14, wherein the conductive layer is selected from the group consisting of a metal, metal alloy and metal compound.

22. The semiconductor circuit fuse of claim 14, wherein the conductive layer comprises tungsten silicide.

23. The semiconductor circuit fuse of claim 14, including configuring the refractory metal nitride layer and the conductive layer to a similar shape.

24. The semiconductor circuit fuse of claim 23, wherein the similar shape comprises a neck portion located between terminal portions.

25. The semiconductor circuit fuse of claim 24, wherein the neck portion is smaller in width than the terminal portions.

26. The semiconductor circuit fuse of claim 25, wherein the neck portion has a width within a range of about 0.2 to about 1 micron.

27. The semiconductor circuit fuse of claim 26, wherein the width of the neck portion is about 0.35 microns.

28. The semiconductor circuit fuse of claim 27, wherein a length of the neck portion is within a range of about 1 to about 10 microns.

29. The semiconductor circuit fuse of claim 28, wherein the length of the neck portion is about 3.5 microns.

30. A method of using a fuse in an integrated circuit, comprising:

providing a fuse containing a conductive layer and a refractory metal nitride layer disposed above an insulating substrate and having a neck portion extending between terminal portions, the neck portion having a width of about 0.35 microns; and

applying electrical current between the terminal portions sufficient to blow the fuse by causing the neck portion of the conductive layer to melt.

31. The method of claim 30, including providing the neck portion with a length of about 3.5 microns.

32. The method of claim 30, including applying an electrical current within a range of about 1 to about 25 mA.

33. The method of claim 30, including applying an electrical current of about 5.5 mA.

34. A method of using a fuse in an integrated circuit, comprising:

providing a fuse containing a conductive layer and a refractory metal nitride layer disposed above an insulating substrate and having a neck portion extending between terminal portions; and

applying electrical current within a range of about 1 to about 25 mA between the terminal portions sufficient to blow the fuse by causing the neck portion of the conductive layer to melt.

35. The method of claim 34, including providing the neck portion with a length of about 3.5 microns.

36. The method of claim 34, including providing the neck portion with a length of about 0.35 microns.

37. The method of claim 34, including applying an electrical current of about 5.5 mA.